Amendments to the Specification:

Please replace the paragraph beginning at page 2, line 17, with the following rewritten paragraph:

FIG. 1 illustrates a silicon-on-insulator (SOI) wafer 100 with shallow tench isolation regions formed using the conventional methods just described. In this figure, a silicon substrate 102 supports a buried oxide layer 104 and a SOI layer 106. In four active areas ~~120 - 126~~ 120, 122, 124, 126, a pad oxide layer 108 and pad nitride layer 110 cover the SOI layer 106. Three trenches are formed between the active areas ~~120 - 126~~ 120, 122, 124, 126 and are filled [[will]] with an electrically-insulative oxide such as silicon dioxide 112. Because the silicon dioxide 112 is thermally grown using a CVD process, the silicon dioxide 112 in each trench includes seams 114 where growth fronts met when the silicon dioxide 112 was being formed. Furthermore, FIG. 1 depicts the over and under polishing that occurs when a thick layer of silicon dioxide 112 must be planarized over the entire surface of the wafer 100. For example, the right-side of the wafer 100 shows that the planarization step removed silicon dioxide 112 from the trench while the left-side of the wafer 100 shows that some silicon dioxide 112 still remains on the pad nitride layer 110.